

## CLAIMS

### WHAT IS CLAIMED IS:

- 1           1.     A method of manufacturing an integrated circuit having  
2     trench isolation regions in a substrate including germanium, the method  
3     comprising:  
4                 forming a mask layer above the substrate;  
5                 selectively etching the mask layer to form apertures  
6     associated with locations of the trench isolation regions;  
7                 forming trenches in the substrate at the locations;  
8                 providing a semiconductor or metal layer by selective  
9     epitaxial growth; and  
10                forming oxide liners using the semiconductor or metal layer  
11    in the trenches of the substrate.
- 1           2.     The method of claim 1, further comprising providing an  
2     insulative material in the trenches to form the trench isolation regions.
- 1           3.     The method of claim 2, further comprising removing the  
2     insulative material until the mask layer is reached.
- 1           4.     The method of claim 1, further comprising:  
2                 providing a low temperature process oxide layer above the  
3     substrate and an amorphous capping layer above the oxide layer.
- 1           5.     The method of claim 1, wherein the amorphous capping layer  
2     is amorphous silicon.
- 1           6.     The method of claim 1, wherein the semiconductor or metal  
2     layer includes silicon material.

1           7.     The method of claim 1, further comprising:  
2                     providing a silicon nitride layer above the substrate and  
3     providing an amorphous capping layer above the silicon nitride layer.

1           8.     The method of claim 1, wherein the forming oxide liners step  
2     is an oxidation process.

1           9.     A method of forming shallow trench isolation regions in a  
2     strained semiconductor layer, the method comprising:  
3                     providing a hard mask layer above the semiconductor layer;  
4                     providing a photoresist layer above the hard mask layer;  
5                     selectively removing portions of the photoresist layer at  
6     locations in a photolithographic process;  
7                     removing the hard mask layer at the locations;  
8                     forming trenches in the hard mask layer under the locations;  
9                     providing a conformal semiconductor layer in the trenches;  
10    and  
11                    oxidizing to form a liner in the trenches.

1           10.    The method of claim 9, further comprising:  
2                    providing a pad oxide layer above a strained silicon layer  
3     before the providing a hard mask layer step.

1           11.    The method of claim 10 further comprising:  
2                    removing the pad oxide layer at the locations before the  
3     forming trenches step.

1           12.    The method of claim 9, further comprising:  
2                    providing an insulative material in the trenches to form the  
3     shallow trench isolation regions; and  
4                    removing the hard mask layer in a wet bath.

- 1           13.    The method of claim 9, further comprising:  
2                    providing a germanium-containing layer above the strained  
3   semiconductor layer.
- 1           14.    The method of claim 13, wherein the strained semiconductor  
2   layer is at least 200 Å thick.
- 1           15.    The method of claim 14, wherein the germanium-containing  
2   cap layer is 100 Å –400 Å .
- 1           16.    The method of claim 15, wherein the oxide liner is silicon  
2   dioxide grown in an oxygen atmosphere.
- 1           17.    A method of forming a liner in a trench in a germanium  
2   containing layer, the method comprising:  
3                    selectively etching the germanium containing layer to form  
4   the trench;  
5                    providing a semiconductor layer in the trench; and  
6                    forming an oxide liner from the semiconductor layer.
- 1           18.    The method of claim 17, wherein the semiconductor layer is  
2   provided by epitaxial growth, the epitaxial growth bears a deposition  
3   process performed at a temperature below 600°C.
- 1           19.    The method of claim 17, wherein the semiconductor layer is  
2   provided in a epitaxy process, a chemical vapor deposition process or  
3   molecular beam.
- 1           20.    The method of claim 19, wherein the oxide liner is  
2   100-200 Å thick.